

#5 03 CD



I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on February 15, 2002.

*Hugh H. Matsubayashi* 2/15/02  
Hugh H. Matsubayashi Date of Signature

Attorney Docket No.: P5826 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Whay S. Lee and Thomas M. Mortensen  
Group Art Unit: unassigned  
Examiner's Name: unassigned

Application No.: 09/967,142

Filing Date: September 28, 2001

For: Discovery of Nodes in an Interconnection Fabric

Commissioner for Patents  
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. §§ 1.56, 1.97, and 1.98

Sir:

In accordance with the duty of disclosure imposed by 37 C.F.R. §§ 1.56, 1.97, and 1.98, Attorneys for Applicant hereby invite the Examiner's attention to the references listed on the accompanying revised PTO Form 1449 entitled "Information Disclosure Statement by Applicant."

Identification of references listed on the accompanying PTO Form 1449 is not to be construed as an admission of Applicant or Attorneys for Applicant that such references are available as prior art against the subject application. Further, the right is reserved to antedate any included reference in accordance with standard procedure.

This submission is understood to complement the results of the Examiner's own independent search. The submission should not be construed as a representation that a search was made or that the cited references are

inclusive of all the relevant and material citations that may be available publicly.

X Copies of each cited publication and U.S. and foreign patent are submitted herewith, along with a concise explanation of foreign language publications (if any).

Applicant respectfully requests that the listed references be considered by the Examiner and be made of record in the application identified above. The Examiner is requested to initial and return the enclosed PTO Form 1449 in accordance with MPEP § 609.

X 37 C.F.R. § 1.97(b). No fee is believed due with this statement, because (check all that apply):

- ☐ (1) It is being filed within 3 months of the application filing date; OR
- ☐ (2) It is being filed within 3 months of entry of a national stage; OR
- ☒ (3) It is being filed before the mailing date of the first Office Action on the merits.

Respectfully submitted,



Hugh H. Matsubayashi  
Attorney for Applicant  
Reg. No.: 43,779  
Phone: (510) 936-2733

**Form PTO-1449** (modified)  
List of Patents and Publications  
For Applicant's Information  
Disclosure Statement  
(Use several sheets if necessary)

ATTY. DKT. NO.: P5826 US

SERIAL NO.: 09/967,142

APPLICANTS: Lee et al.

GROUP: unknown

FILING DATE: September 28, 2001

**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	6,016,510	1/18/00	Quattromani, et al.			
	A2	6,023,753	2/8/00	Pechanek, et al.			
	A3	5,689,661	11/18/97	Hayashi, et al.			
	A4	6,167,502	12/26/00	Pechanek, et al.			
	A5	6,101,181	8/8/00	Passint, et al.			
	A6	5,720,025	2/17/98	Wilkes, et al.			
	A7	5,970,232	10/19/99	Passint, et al.			
	A8	6,055,618	4/25/00	Thorson			
	A9	5,701,416	12/23/97	Thorson, et al.			
	A10	5,737,628	4/7/98	Birrittella, et al.			
	A11	5,689,646	11/18/97	Thorson			

**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	A12	99/26429	5/27/99	WO			
	A13	0 785 512	7/23/97	EP			

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

	A14	Bradley Kuszmaul, Mercury Computer Systems, Inc., "The RACE Network Architecture," (posted at <a href="http://www.mc.com/techlit/#tech_brief">www.mc.com/techlit/#tech_brief</a> prior to this), 6 pages.
	A15	R.Y. Wang, T.E. Anderson and D.A. Patterson, "Virtual Log Based File Systems For a Programmable Disk," Proc. Third Symposium on Operating Systems Design and Implementation, February 1999 (Also appeared as University of California Technical Report CSD-98-1031, 16 pages.
	A16	Prasant Mohapatra, "Wormhole Routing Techniques for Directly Connected Multicomputer Systems, ACM Computing Surveys, Vol. 30, No. 3, September 1998, 37 pages.
	A17	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Journal of the Association for Computing Machinery, Vol. 41, No. 5, September 1994, pp. 874-902.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

**Form PTO-1449** (modified)  
List of Patents and Publications  
For Applicant's Information  
Disclosure Statement  
(Use several sheets if necessary)

ATTY. DKT. NO.: P5826 US

SERIAL NO.: 09/967,142

APPLICANTS: Lee et al.

GROUP: unknown

FILING DATE: September 28, 2001

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

A18	Reddy, Dept. of Computer & Information Sciences, "A Dynamically Reconfigurable WDM LAN Based on Reconfigurable Circulant Graph," IEEE, 1996, 4 pages.
A19	Funahashi, Jouraku and Amano, "Adaptive Routing for Recursive Diagonal Torus," Transactions of the Institute of Electronics, Information and Communication Engineers D-I, vol. J83D-I, no. 11, November 2000, pp. 1143-53.
A20	Milan Kovacevic, Center for Telecommunications Research, "On Torus Topologies with Random Extra Links," IEEE 1996, pp. 410-418.
A21	Dally, et al., The Torus Routing Chip, Distributed Computing, Springer-Verlag 1986, pp. 187-196.
A22	Susan Hinrichs, "A Compile Time Model for Composing Parallel Programs," IEEE Parallel and Distributed Technology, 1995, 19 pages.
A23	"CRAY T3D System Architecture Overview Manual," <a href="ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html">ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html</a> , Cray Research, 1993, 40 pages.
A24	Marco Fillo, et al., "The M-Machine Multicomputer," Laboratory for Computer Science, Massachusetts Institute of Technology, A.I. Memo No. 1532, Ann Arbor, March 1995, 14 pages.
A25	Noakes, et al., "The J-Machine Multicomputer: An Architectural Evaluation," Proceedings of the 20 <sup>th</sup> International Symposium on Computer Architecture, May 1993, 12 pages.
A26	Dally, et al., "Architecture of a Message-Driven Processor," International Conference on Computer Architecture, June 1987, pp. 189-196.
A27	Dennison, Lee and Dally, "High-Performance Bidirectional Signalling in VLSI," Massachusetts Institute of Technology, October 12, 1992, 20 pages.
A28	Dally, et al., "Architecture and Implementation of the Reliable Router," Mass. Institute of Technology, Proceedings of Hot Interconnects II, Stanford CA, August 1994, 12 pages.
A29	Dally, et al., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers," Proceedings of the First International Parallel Computer Routing and Communication Workshop, Seattle WA, May 1994, 15 pages.
A30	Dennison, et al., "Low-Latency Plesiochronous Data Retiming," Mass. Institute of Technology, Proceedings of the 1995 Advanced Research in VLSI Conference, Chapel Hill NC, March 1995, 12 pages
A31	Whay S. Lee, "Mechanism for Efficient, Protected Messaging," Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, January 20, 1999, 147 pages.
A32	Dennison, "Reliable Interconnect Networks for Parallel Computers," Mass. Institute of Technology, Dept. of Electrical Engineering and Computer Science, April 18, 1991, 79 pages.
A33	Thucydides Xanthopoulos, "Fault Tolerant Adaptive Routing in Multicomputer Networks," Dept. of Electrical Engineering and Computer Science, Mass. Institute of Technology, January 20, 1995, 152 pages.
A34	Dennison, "The Reliable Router: An Architecture for Fault Tolerant Interconnect," Dept. of Electrical Engineering and Computer Science, Mass Institute of Technology, May 24, 1996, 145 pages.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

# U.S. PATENT DOCUMENTS

**OTHER ART** (Including Author, Title, Date, Pertinent Pages, Etc.)

A35	"Introduction To Parallel Algorithms and Architectures: Arrays, Trees, Hypercubes," F. Thomson Leighton, Morgan Kaufmann Publishers, 1992, pp. 1-831.
-----	---

	A36	Christopher J. Glass and Lionel Ni, "Fault-Tolerant Wormhole Routing in Meshes," Technical Report, MSU-CPS-ACS-72, October 30, 1992 (revised May 25, 1993), 28 pages.
--	-----	---

A37	Stefan Savage and John Wilkes, "AFRAID—A Frequently Redundant Array of Independent Disks," Proceedings of the 1996 USENIX Technical Conference, pp. 27–39, San Diego, CA, January 1996, 13 pages.
-----	---

	A38	Steve Ward, et al., "A Modular, Scalable Communications Substrate," MIT Laboratory for Computer Science, July 1993, 10 pages.
--	-----	---

A39	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Technical Reports, MSU-CPS-ACS-44, October 10, 1991 (revised March 2, 1992), pages 278-287 (numbered herein as 1-20).
-----	---

A40	Thomas Stricker, "Message Routing on Irregular 2D-Meshes and Tori," School of Computer Science, Carnegie Mellon Univ., January 15, 1991, pages 170-177 (numbered herein as 1-19).
-----	---

	A41	Dally, et al., "The J-Machine: A Restrospective," in 25 Years of the International Symposia on Computer Architecture – Selected Papers. Pp. 54–58
--	-----	---


[illegible]

--	--	--

--	--	--

--	--	--

[illegible]


[illegible]



[illegible]


[illegible]


--	--	--

EXAMINER: \_\_\_\_\_ DATE CONSIDERED: \_\_\_\_\_

EXAMINER: Initial if citation considered whether or not citation is in conformance with MPER 600; Draw line through citation if

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609, Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

